		IEEE iNIS 2015 Program Outline	
21-Dec-15	11:00-11:30	Registration at Radisson Blu Hotel Indore	
	11:30-12:30	Inaugural Event at Radisson Blu Hotel Indore	
	12:30-14:00	Lunch at Radisson Blu Hotel Indore	
	14:00-15:00	Keynote # 1 Managing Large Health Care Data Dharma P. Agrawal University of Cincinnati, Cincinnati, OH, USA	
	15:00-16:00	Session 01: Reliability and Security Aware RTL/System Design for Application Specific Hardware Accelerators	Session 02: Emerging Nanoelectronic Devices - Design and Characterization
	16:00-17:00	Session 03: Memory and Computing Units in Emerging Paradigm	Session 04: Energy Efficient WSN
	17:00-18:00	Session 05: Multicore System Simulation using Graphite 1000 cores Simulator	Session 06: Information Processing Applications
	18:00-19:00	Photo Session and Break	
	19:00-21:00	Welcome Dinner (Including IEEE Outreach) at Radisson Blu Hotel Indore	
22-Dec-15	8:00-8:30	Registration at Radisson Blu Hotel Indore	Tea/Coffee
	8:30-9:30	Keynote # 2 Spot Defect Modeling: History and Perspectives Michel Renovell University of Montpellier, Montpellier, France	
	9:30-10:30	Session 07: Reliability and Energy Aware RTL Design for System-on-Chip	Session 08: Power Aware Design
	10:30-11:30	Session 09: Unconventional Computing	Session 10: High Performance Architecture and System Design
	11:30-12:30	Session 11: Mitigating the Dark Silicon Phenomenon on Next-Generation Network Processor Architectures	Session 12: Advanced Memory and Digital Systems Design
	12:30-13:45	Lunch at Radisson Blu Hotel Indore	
	13:45- 14:45	Keynote #3 Solving Big-Data problems with Automata Computing Mircea Stan University of Virginia, Charlottesville, VA	
	14:45-15:45	Session 13: Doping and junction free transistors for future computing	Session 14: Energy Efficient VLSI Systems
	15:45-16:00	Tea/Coffee	

	16:00-17:00	Session 15: Graphene based Interconnects for the Post-CMOS Era	Session 16: Low Power Design
	17:00-18:00	Session 17: Cloud Resource Management in the Big Data and Internet of Things Era	Session 18: IOT Applications I
	18:00-19:00	Photo Session and Break	iNIS Committee Meeting
	19:00-21:00	Banquet Dinner at Radisson Blu Hotel Indore	
	8:00-8:30	Registration at Radisson Blu Hotel Indore	Tea/Coffee
	8:30-9:30	Keynote # 4 Improving Yield and Reliability of Chip Multiprocessors in Nanotechnology Sandip Kundu University of Massachusetts, Amherst, MA	
	9:30-10:30	Session 19:Modeling and Design Challenges of Three Dimensional Integration in Neuromorphic Circuits	Session 20: IOT Applications II
23-Dec-15	10:30-11:30	Session 21: Smart and Secure System Design	Session 22: Emerging Nanoelectronic Materials and Devices
	11:30-12:30	Session 23: Energy Efficient System Design	Session 24: Advanced Sensor Design
	12:30-13:45	Lunch at Radisson Blu Hotel Indore	
	13:45- 14:45	Session 25: High Performance Computing Systems	Session 26: Emerging Nanoelectronic Materials and Systems II
	14:45-15:45	Session 27:Trustworthy System Design	Session 28: Big Data Analysis and Performance Optimization
	15:45-16:30	Awards and Closing Ceremony	

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	14:00-15:00	**Keynote # 1 Managing Large Health Care Data** **Dharma P. Agrawal** **University of Cincinnati, Cincinnati, OH, USA** **Chair: Saraju P. Mohanty, University of North Texas, USA**	
	15:00-16:00	**Session 01:** Reliability and Security Aware RTL/System Design for Application Specific Hardware Accelerators **Chair: Anirban Sengupta, Indian Institute of Technology, Indore, India**	**Session 02:** Emerging Nanoelectronic Devices - Design and Characterization **Chair: Anurag Srivastava, ABV-IIITM, Gwalior, India**
		Secure Information Processing during System-Level: Exploration of an Optimized Trojan Secured Datapath for CDFGs during HLS based on User Constraints; Anirban Sengupta, Saumya Bhadauria	**Clocked Adiabatic XOR and XNOR CMOS Gates Design Based on Graphene Nanoribbon Complementary Field Effect Transistors**; Yaser Banadaki, Ashok Srivastava and Safura Sharifi
		Energy Aware Synthesis of Application Kernels expressed in Functional Languages on a Coarse Grained Composable Reconfigurable Array; Nalesh S, Saptarsi Das, Kavitha Madhu, S. K. Nandy	**Performance Enhancement of Dopingless Tunnel-FET based on Ge-source with High-k Dielectric**; Kanchan Cecil and Jawar Singh
	16:00-17:00	**Session 03:** Memory and Computing Units in Emerging Paradigm **Chair: Himanshu Thapliyal, University of Kentucky, USA**	**Session 04:** Energy Efficient WSN **Chair: Manisha Pattnaik, ABV-IIITM, Gwalior, India**
		Designing Nanoelectronic-compatible 8-bit Square Root Circuit by Quantum-dot Cellular Automata; Mohammad Reza Jahangir, Shadi Sheikhfaal, Shaahin Angizi, Keivan Navi, Firdous Ahmad	**Robust Energy Efficient Multipath Routing Protocol for Wireless Sensor Networks**; Prasun Seal, Tuhina Samanta and Mainak Chatterjee

21-Dec-15		Nanoscale Memory Design for Efficient Computation: Trends, Challenges and Opportunity; Santosh Kumar Vishvakarma	Energy-saving image transmission over WMSN using block size reduction technique; Tamal Pal, Shaon Bandyopadhyay and Sipra Dasbit
			At a glance of sybil detection in OSN; Krishna Kansara, Narendra Shekokar
	17:00-18:00	Session 05: Multicore System Simulation using Graphite 1000 cores Simulator Chair: Prasun Ghosal, Indian Institute of Engineering Science and Technology, India	Session 06: Information Processing Applications Chair: Kamalakanta Mahapatra, NIT, Rourkela, India
		Multicore ICs: Recent Trends in Developing Methodologies and Frameworks for Simulation; Prasun Ghosal, Soumyajit Poddar	Robustness analysis of a digital image watermarking technique for various frequency bands in DCT domain; Shabir Parah, Shazia Ashraf, Ayaash Ashraf
			Gradient Descent with Momentum based Neural Network Pattern Classification for the Prediction of Soil Moisture Content in Precision Agriculture; Saroj Lenka, Ambarish Mohapatra
			Twitter Sentimental Analysis - A more enhanced way of classification and scoring; Sanket Sahu, Suraj Kumar Rout, Debasmit Mohanty
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	8:00-8:30	Registration at Radisson Blu Hotel Indore	Tea/Coffee
	8:30-9:30	**Keynote # 2 Spot Defect Modeling: History and Perspectives** **Michel Renovell** **University of Montpellier, Montpellier, France** **Chair: Dhruva Ghai, Oriental University, India**	
	9:30-10:30	**Session 07:** **Reliability and Energy Aware RTL Design for System-on-Chip Chair: Anirban Sengupta, Indian Institute of Technology, Indore, India**	**Session 08:** **Power Aware Design Chair: Manisha Pattnaik, ABV-IIITM, Gwalior, India**
		A Reliable Digitally Synthesizable Linear Drop-out regulator design for 14nm SOC; Pradipta Patra, Ramnarayanan Muthukaruppan, Sumedha Mangal	**Circuit Implementation of Switchable Pins in Chip Multiprocessor;** Zhou Zhao, Ashok Srivastava, Lu Peng, Shaoming Chen and Saraju P. Mohanty
		Intelligent Vision Systems: Exploring the State-of-the-Art and Opportunities for the Future; Siddharth Advani, Srinidhi Kestur, Vijay Narayanan,	**Power Minimization of a Memristor-Based Wien Bridge Oscillator through a Simscape Framework: A Memristor-Oscillator Power Minimization Case Study;** Prasun Ghosal and Saraju P. Mohanty
	10:30-11:30	**Session 09: Unconventional Computing Chair: Himanshu Thapliyal, University of Kentucky, USA**	**Session 10: High Performance Architecture and System Design Chair: Prasun Ghosal, Indian Institute of Engineering Science and Technology, Shibpur, India**
		Fast Qubit Placement in 2D Architecture using Nearest Neighbor Realization; Ritu Ranjan Shrivastwa, Kamalika Datta, Indranil Sengupta	**Reconfigurable Concurrent VLSI(FPGA) Design Architecture of CRC-32 for high-speed data communication;** Jubin Mitra and Tapan Kumar Nayak
		Synthesis of Vertex Coloring Problem using Grover's Algorithm; Amit Saha, Avik Chongder, Sudhindu Bikash Mandal, Amlan Chakrabarti	**FPGA Prototype of Low Latency BBS PRNG;** Amit Kumar Panda and Kailash Chandra Ray
		Design of Testable Adder Circuits for Spintronics Based Nanomagnetic Computing; Carson Labrado, Himanshu Thapliyal, Ronald DeMara	

22-Dec-15	11:30-12:30	**Session 11:** Mitigating the Dark Silicon Phenomenon on Next-Generation Network Processor Architectures **Chair: Sourav Roy, Freescale, India** **Mitigating the Dark Silicon Phenomenon on Next-Generation Network Processor Architectures;** Sourav Roy	**Session 12:** Advanced Memory and Digital Systems Design **Chair: Debasmit Mohanty, StratLytics** **Simulation based Performance Study of Cache Coherence Protocols;** Neethu Mallya, Geeta Patil and Biju Raveendran **Test Time Optimization for 3D - SICs Having Multiple Towers;** Chandan Giri, Sumit Dhuwalia, Nikhil Khemka, Prince Gupta and Surajit Kumar Roy
	12:30-13:45	Lunch at Radisson Blu Hotel Indore	
	13:45- 14:45	**Keynote #3 Solving Big-Data problems with Automata Computing** **Mircea Stan** **University of Virginia, Charlottesville, VA** **Chair: Saraju P. Mohanty, University of North Texas, USA**	
	14:45-15:45	**Session 13:** Doping and junction free transistors for future computing **Chair: Jawar Singh, Indian Institute of Information Technology, India** **Extended Base Schottky-collector Bipolar Charge Plasma Transistor:** Lokesh Kumar Bramhane, Jawar Singh	**Session 14:** Energy Efficient VLSI Systems **Chair: Anurag Srivastava, ABV-IIITM, Gwalior, India** **Energy Efficient Analog-to-Information Converter For Biopotential Acquisition Systems;** Wazir Singh and Sujay Deb **ZMesh: An Energy-Efficient Network-on-Chip Topology for Constant-Geometry Algorithms;** N Prasad, Santanu Chattopadhyay and Indrajit Chakrabarti **FinFETs and their application as load switches in micromechatronics;** Sreeja Nair and Mary Regeena
	15:45-16:00	Tea/Coffee	

		Session 15: Graphene based Interconnects for the Post-CMOS Era Chair: Rohit Sharma, Indian Institute of Technology, Ropar, India	Session 16: Low Power Design Chair: Mary Regeena, BITS-Pilani, Dubai
	16:00-17:00	**Accurate Numerical Model for Crosstalk Analysis of SWCNT Bundle Interconnects Using FDTD Method;** Vobulapuram Ramesh Kumar, Brajesh Kumar Kaushik and Amalendu Patnaik	**Generalized Optimum Reversible Circuit Synthesis: A Memetic Approach;** Roshni Chakraborty and Prasun Ghosal
		Correlating Chemical Structure and Charge Transport in Reduced Graphene Oxide for Transparent Conductor and Interconnect Applications; Vikas Rai, M K Kavitha and Manu Jaiswal	**A 120 nW, Tunable, PVT Invariant Voltage Reference with 80 dB Supply Noise Rejection;** Nirmoy Modak, Baibhab Chatterjee, Anvesha Amaravati and Maryam Shojaei Baghini
		Performance Analysis of AsF5-intercalated Top-Contact MultiLayer Graphene NanoRibbon Interconnects; Atul Kumar Nishad and Rohit Sharma	
	17:00-18:00	Session 17: Cloud Resource Management in the Big Data and Internet of Things Era Chair: Rajiv Ranjan, Newcastle University	Session 18: IOT Applications I Chair: Ajay Gadicha, PRP College of E&T, Amravati, India
		Orchestrating Quality of Service in the Cloud of Things Ecosystem: Prem Prakash Jayaraman, Karan Mitra, Saguna Saguna, Tejal Shah, Dimitrios Georgakopoulos, Rajiv Ranjan	**A Smart Gym Framework: Theoretical Approach;** Abhay Jain
			An IoT-Enabled Modular Quadrotor Architecture for Real-Time Aerial Object Tracking; Gavin Coelho, Elias Kougianos, Saraju P. Mohanty, Prabha P. Sundaravadivel, and Umar Albalawi
	18:00-19:00	Photo Session and Break	iNIS Committee Meeting
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	8:30-9:30	**Keynote # 4 Improving Yield and Reliability of Chip Multiprocessors in Nanotechnology** **Sandip Kundu** **University of Massachusetts, Amherst, MA** **Chair: Dhruva Ghai, Oriental University, India**	
	9:30-10:30	**Session 19:Modeling and Design Challenges of Three Dimensional Integration in Neuromorphic Circuits** **Chair: Yiyu Shi, University of Notre Dame, USA**	**Session 20: IOT Applications II** **Chair: Ajay Gadicha, PRP College of E&T, Amravati, India**
		Three Dimensional Integration Technology Applied to Neuromorphic Hardware Implementation; M. Ehsan, Zhen Zhou, Yang Yi	**Smart Dietary Monitoring System;** Javaid Nabi, Abhijit Rd and Raghav Lakhotia
			Remote Surveillance Robot System- A Robust Framework using Cloud; Aditya Sundaram, Monel Gupta and K Chandrasekaram
			Enabling Context-Aware Computing in Internet of Things using M2M; Prateek Anand
	10:30-11:30	**Session 21: Smart and Secure System Design** **Chair: Kamalakanta Mahapatra, NIT, Rourkela, India**	**Session 22: Emerging Nanoelectronic Materials and Devices** **Chair: Mary Regeena, BITS-Pilani, Dubai**
		Area, Energy, and Time Assessment for a Distributed TPM for Distributed Trust in IoT Clusters; Hala Hamadeh, Soma Chaudhuri and Akhilesh Tyagi	**Effect of Gate and Channel Engineering on Digital Performance Parameters using Tied (3T) and Independent (4T) Double Gate MOSFETs;** Neha Jagwani, Santosh Kumar Vishvakarma and Vikas Vijayvargiya
		An Approach to A University Recommendation by Multi-Criteria Collborative Filtering and Dimensionality Reduction Techniques; Debajyoti Mukhopadhyay, Sheetal Girase and Dheeraj Kumar Bokde	**NH3 adsorption on Arsenene: A First principle study;** Md. Shahzad Khan, Venakatesh Ranjan and Anurag Srivastava
		Comparator Mining Lead To Better Alternatives For Making Better Decision; Priyanka Shirsath and Ujwala Patil	**Shape dependent structural stability, electronic and optical properties of CdO nanowire;** Rajneesh Chaurasiya, Md. Shahzad Khan and Anurag Srivastava
23-Dec-15		**Session 23: Energy Efficient System Design** **Chair: Jawar Singh, IIIT, Jabalpur, India**	**Session 24: Advanced Sensor Design** **Chair: Ashok Srivastava, Louisiana State University, USA**

	11:30-12:30	**Design and Analysis of Rectangular Microstrip Patch Antenna for ZigBee Applications;** Sanya Srivastava and Devendra Somwanshi	**Carbon Nanotube based NH3 Gas Sensor: Ab-initio Study;** Sushmita Dandeliya and Anurag Srivastava
		Base Station Controlled and Energy Efficient Centralized Hierarchical Routing Protocol; Shubhanjali Sharma, Vinesh Jain and M.C. Govil	**GO/μ–IDEs/p-Si Based Real Time Sensors for F- Detection in Natural Drinking Water;** Mahesh Soni, Tarun Arora, Pawan Kumar, Ajay Soni and Satinder Kumar Sharma
			2D Colloidal Crystals based SERS Sensors for NH3 Detection; Pawan Kumar and Satinder Kumar Sharma
	12:30-13:45	Lunch at Radisson Blu Hotel Indore	
	13:45- 14:45	**Session 25: High Performance Computing Systems** Chair: Anirban Sengupta, Indian Institute of Technology, Indore, India	**Session 26: Emerging Nanoelectronic Materials and Systems II** Chair: Jawar Singh, IIIT, Jabalpur, India
		Accuracy Configurable modified Booth Multiplier using approximate Adders; Pranay Babu and Srivatsava Jandhyala	**Performance Analysis of Multilayer Graphene Nano-Ribbon in Current-Mode Signaling Interconnect System;** Yash Agrawal, Rajeevan Chandel and Girish Kumar
		Design and Implementation of Quadruple Floating-Point CORDIC; Arun Kumar Singh, Madhav Kumar Singh and Kailash Chandra Ray	**CO Adsorption on In-groupV Zig-Zag Nanowires: First Principles Analysis;** B Santhibhushan, Md Shahzad Khan and Anurag Srivastava
		A Hardware Architecture for Better Portable Graphics (BPG) Compression Encoder; Umar Albalawi, Saraju P. Mohanty and Elias Kougianos	**Timing and Stability Analysis of Carbon nanotube Interconnects;** Girish Kumar, Rajeevan Chandel and Yash Agrawal
	14:45-15:45	**Session 27:Trustworthy System Design** Chair: Kamalakanta Mahapatra, NIT, Rourkela, India	**Session 28: Big Data Analysis and Performance Optimization** Chair: Debasmit Mohanty, StratLytics
		A Novel PUF based SST to Prevent Distribution of Rejected ICs from Untrusted Assembly; Sudeendra Kumar, Hanumantha Rao G, Sauvagya Sahoo and Kamala Kanta Mahapatra	**Dynamic Data Shapers Optimize Performance in Dynamic Binary Optimization (DBO) Environment;** Varun Venkatesan, Swamy Ponpandi and Akhilesh Tyagi
		Modified Configurable RO PUF with Improved Security Metrics; Sauvagya Sahoo, Sudeendra Kumar and Kamala Kanta Mahapatra	**Detection of Diabetic Retinopathy in Retinal Images using MLP classifier;** Amol Bhatkar and Govind Kharat
	15:45-16:30	Awards and Closing Ceremony	